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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/698,186	10/30/2000	Kosuke Inoue	500.39252X00	3559

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EXAMINER

OWENS, DOUGLAS W

ART UNIT PAPER NUMBER

2811

DATE MAILED: 12/04/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/698,186

Applicant(s)

INOUE ET AL.

Examiner

Douglas W Owens

Art Unit

2811

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 02 July 2002.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-38 is/are pending in the application.
- 4a) Of the above claim(s) 1-18 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 19-38 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 30 October 2000 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 7, 8, 13.
- 4) ☐ Interview Summary (PTO-413) Paper No(s) _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election of the invention of group II in Paper No. 12 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Priority

2. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Drawings

3. Figures 31 and 32 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

4. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference characters "5" and "16" have both been used to designate the polyimide layer in Fig. 3, which is called the electric power supply portion in Fig. 4 (See page 24, lines 14-23). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

5. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Objections

6. Claim 23 is objected to because of the following informalities: The phrase "printing by a plurality" should be replaced with "printing a plurality". Appropriate correction is required.

Claim Rejections - 35 USC § 112

7. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. Claims 24, 33 and 34 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 24 recites the limitation, "...said first step of forming...". There is no prior mention of a "first step" in claim 19, which claim 24 depends from.

Claim 33 recites the limitation, "...mask used in said printing...has openings smaller than an area of said second insulating layer." The scope of the claim is vague because it cannot be determined from the claim what area of the second insulating film is larger than the openings.

Claim Rejections - 35 USC § 102

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

10. Claim 19 is rejected under 35 U.S.C. 102(b) as being anticipated by Japanese patent No. JP405175260A to Shirasaki.

Shirasaki teaches a method of producing a semiconductor apparatus comprising a step of forming an electrically insulating layer (17) on a wafer by printing with the use of a mask (18).

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

12. Claims 20 – 32 and 34 – 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over US patent No. 6,313,532 to Shimoishizaka et al. in view of Shirasaki.

Regarding claim 20, Shimoishizaka et al. teaches a method of producing a semiconductor apparatus comprising:

a first step of forming an electrically insulating layer (20) on a wafer;

a second step of forming a wiring (13) over an area from a circuit electrode (11) to an inclined portion and a flat portion of the electrically insulating layer; and

a third step of forming an external connection terminal (40) on the electrically insulating layer so that the external connection terminal is electrically connected with the circuit electrode through the wiring.

Shimoishizaka et al. does not teach printing the electrically insulating layer.

Shimoishizaka et al. is silent with respect to the manner in which the electrically insulating layer is formed. One having ordinary skill in the art would have been required to select a known method of patterning the electrically insulating layer. Shirasaki teaches a known method of patterning a layer, using contact printing. It would have been obvious to one of ordinary skill in the art to employ the method of patterning taught by Shirasaki in the method taught by Shimoishizaka et al. since it is a known method, as explained above.

Regarding claim 21, Shimoishizaka et al. teaches a method of producing a semiconductor apparatus comprising:

- a first step of forming an electrically insulating layer (20) on a wafer;
- a second step of forming a pad (32) on the electrically insulating layer;
- a third step of forming a wiring (13) on the electrically insulating layer so that the wiring layer electrically connects a circuit electrode (11) of the wafer with the pad; and
- a fourth step of forming an external connection terminal (40) on the pad.

Shimoishizaka et al. does not teach printing the electrically insulating layer.

Shimoishizaka et al. is silent with respect to the manner in which the electrically insulating layer is formed. One having ordinary skill in the art would have been required to select a known method of patterning the electrically insulating layer. Shirasaki teaches a known method of patterning a layer, using contact printing. It would have been obvious to one of ordinary skill in the art to employ the method of patterning taught

by Shirasaki in the method taught by Shimoishizaka et al. since it is a known method, as explained above.

Regarding claims 22 and 30, Shimoishizaka et al. does not teach a method, wherein the electrically insulating layer contains particles. It would have been obvious to one of ordinary skill in the art to select an electrically insulating material having low elasticity and containing particles, since many such materials, including resins, are known that would have been well suited for the intended use. The selection of a known material based on its suitability for its intended use supported a *prima facie* obviousness determination in *Sinclair & Carroll Co. v. Interchemical Corp.*, 325 U.S. 327, 65 USPQ 297 (1945).

Regarding claim 23, Shimoishizaka et al. does not teach a method, wherein the electrically insulating layer is formed by repeating printing steps. It is not considered inventive to duplicate process steps unless a new and unexpected result is achieved.

Regarding claim 24, Shimoishizaka et al. does not teach a method, wherein the first step is performed in a manner so that a squeegee is moved over an opening of the mask from a vertex to an opposite vertex. Shirasaki teaches a method of patterning a layer, wherein a squeegee is moved over an opening of the mask from a vertex to an opposite vertex. It would have been obvious to one of ordinary skill in the art to incorporate the teaching of Shirasaki into the method taught by Shimoishizaka et al. for reasons discussed above.

Regarding claim 25, Shimoishizaka et al. teaches a method as discussed above, and further comprising:

wherein the wafer has a circuit electrode (11);

wherein said step of forming an electrically insulating layer comprises forming a first electrically insulating layer (12) with a part of the circuit electrode exposed;

wherein the electrically insulating layer forming step includes a step of forming a second electrically insulative layer (20) thicker than the first insulating layer;

wherein a wiring (13) in connection to the circuit electrode is formed on the second insulating layer.

Shimoishizaka et al. does not teach forming the electrically insulating layers by printing. Shirasaki teaches a method of forming an insulative layer by printing. It would have been obvious to one of ordinary skill in the art to incorporate the teaching of Shirasaki into the method taught by Shimoishizaka et al. for reasons discussed above.

Regarding claim 26, Shimoishizaka et al. teaches a method wherein the second insulating layer has a thickness of 10 to 150 microns (Col. 7, lines 4 – 6), which includes the entire range of the claimed invention.

Regarding claim 27, Shimoishizaka et al. teaches a method, wherein the second insulating layer has an inclined portion.

Regarding claim 28, Shimoishizaka et al. does not explicitly teach a method, wherein the inclined portion has a 5 to 30 percent gradient. It would have been obvious to one of ordinary skill in the art to arrive at the optimal gradient through routine experimentation.

Regarding claim 29, Shimoishizaka et al. does not teach a method the second insulating layer is a polyimide paste. It would have been obvious to one of ordinary skill

in the art to select polyimide paste, since it is a known material that is well suited for the intended use.

Regarding claims 31 and 32, Shimoishizaka et al. does not teach a method, wherein the second insulating layer is formed with a thermosetting resin and heating. It would have been obvious to one of ordinary skill to select thermosetting resin since it is a known material that is well suited for the intended use. The thermosetting resin would have required a heating step.

Regarding claim 34, Shimoishizaka et al. does not teach a method, wherein the printing of the second insulating film is performed by:

- aligning said mask and pattern with each other;

- filling a resin into openings in the mask by moving a squeegee on the mask; and
- separating the mask from the wafer.

Shirasaki teaches a method of forming a pattern, as recited above. It would have been obvious to one of ordinary skill in the art to incorporate the teaching of Shirasaki into the method taught by Shimoishizaka et al. for reasons discussed above.

Regarding claim 35, Shimoishizaka et al. teaches a method further comprising the step of forming an external connection terminal connected to said wiring.

Regarding claim 36, Shimoishizaka et al. teaches a method, further comprising the step of forming a third electrically insulating layer (50) covering the second insulating layer and wiring.

Regarding claim 37, Shimoishizaka et al. teaches a method, further comprising the step of forming a surface protective layer (50) covering the second insulating layer and wiring.

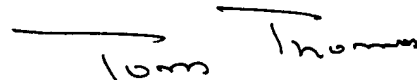
Regarding claim 38, Shimoishizaka et al. teaches a method, further comprising the step of dicing the wafer (Col. 12, lines 34 – 36).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Douglas W Owens whose telephone number is 703-308-6167. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 703-308-2772. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

A handwritten signature in black ink that reads "Tom Thomas". The signature is written in a cursive style with a horizontal line above the name.

DWO
December 1, 2002

TOM THOMAS
SUPERVISOR
EXAMINER
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